



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

CR

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,857	08/23/2002	Vincent K. Chan	00100020042	4596
29153	7590	02/25/2004	EXAMINER	
ATI TECHNOLOGIES, INC. C/O VEDDER PRICE KAUFMAN & KAMMHOLZ 222 N. LASALLE STREET CHICAGO, IL 60601			TRAN, THANH Y	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,857

Applicant(s)

CHAN, VINCENT K.

Examiner

Thanh Y. Tran

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2003.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-26 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 is unclear as to what Applicant means by “wherein the plurality of second solder balls further create a control solder joint when the heat having a temperature greater than or equal to the first melting temperature but less than the second melting temperature is applied, wherein the control solder joint includes a melted outer layer of first material and the second solder ball having the second diameter?

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-7, 15-16 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dockerty et al (U.S. 5,796,169) in view of Matthies et al (U.S. 6,527,159).

With respect to claim 1, Dockerty et al discloses a carrier substrate (1, Fig. 1) comprising a plurality of first solder members (12) having a first solder dimension and a first melting temperature (low melting temperature) disposed on the carrier substrate (1), and a plurality of second members (11) having a second member dimension and a second melting temperature (high melting temperature) disposed on the carrier substrate (1) in a corresponding relationship to the first plurality of solder members (12), wherein the first solder dimension is greater than the second member dimension and the second melting temperature is greater than the first melting temperature (see Fig. 1, col. 3, lines 48-67) and the second members. It should be noted that: since figure 1 shows that the length of contacts (2) is greater than the length of contacts (4), thus the dimension of first solder members (12) (corresponding to contacts 2) is considered greater than the dimension of second solder members.

Dockerty et al does not teach the carrier substrate disposed thereon with a solder dispensing machine and the second members disposed thereon with a solder dispensing machine. However, Matthies et al teaches carrier substrate (10) disposed thereon with a solder dispensing machine (see Figs. 1 and 2, element 14 and 30, col. 2, lines 9-22). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Dockerty et al by using a solder dispensing machine as shown in figure 2 of Matthies et al for the purpose of dispensing the bumps (solder balls) at a very high rate of speed, thus minimizing the time of manufacturer.

With respect to claim 2, Dockerty et al discloses a carrier substrate (1, Fig. 1) wherein the plurality of first solder members (12) and the plurality of second solder members (11) are disposed on a bottom surface of the carrier substrate (1).

With respect to claim 3, Dockerty et al discloses a carrier substrate (1, Fig. 1) further comprising an integrated circuit (3) disposed on the bottom surface of the carrier substrate (1).

With respect to claim 4, figure 5 of Dockerty et al further shows that carrier substrate (24) is capable of being soldered to a printed circuit board (1) and the plurality of second members define a minimum distance between the printed circuit board (1) and substrate (24).

Dockerty et al does not teach that the IC chip is mounted on an opposite side of carrier substrate and facing to the bottom surface of the PCB, so that the plurality of second members define a minimum distance between the printed circuit board and the integrated circuit.

However, the Examiner takes Official Notice that it is known to mount an IC chip on a bottom side of a carrier substrate that faces to the mounting surface of the PCB. Thus, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the reference of Dockerty et al. by replacing the mount of an IC chip on an bottom side of the substrate for the purpose of providing a compact package and also protecting the IC chip when it is mounted on the substrate with the PCB therebetween.

With respect to claims 5, and 18, figure 5 of Dockerty et al further shows that the carrier substrate (24) comprising at least one heat sink (27) disposed on a top surface of the carrier substrate.

With respect to claims 6 and 19, Dockerty et al discloses a carrier substrate (1, Fig. 1) wherein the plurality of second members (11) includes an outer layer of a solder material/first material having the first melting temperature (high melting temperature) (see col. 3, lines 57-60).

With respect to claim 7, Dockerty et al discloses a carrier substrate (1, Fig. 1) wherein the first solder member (12) is composed of a lead tin eutectic alloy (see col. 3, lines 60-63).

With respect to claim 15, it recites limitations similar to claim 1, Dockerty et al further discloses a an integrated circuit (Fig. 5) comprising a carrier substrate (24) having a bottom surface; a printed circuit board (1) having a top surface, and a solder ball array (11, 29) coupling the bottom surface of the carrier substrate (24) to the top surface of the printed circuit board (1). Thus claim 15 is rejected for the same reasons.

With respect to claim 16, it recites limitations similar to claim 4. Therefore, it is rejected for the same reasons.

With respect to claim 20, as best understood, all limitations in claim 20 are considered to read on the references of Dockerty et al and Matthies et al

Method claims 21-22 are deemed to be inherent upon the reference of Dockerty et al and Matthies et al as applied to claims 1-7 and 15-20.

5. Claims 8-14, 17, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dockerty et al (U.S. 5,796,169) in view of Burnette (U.S. 5,956,606).

With respect to claim 8, it recites limitation similar to claim 1, Dockerty et al further teaches that a plurality of first solder paste (12) composed of a first material (lead tin) (see col. 3, lines 60-63). Dockerty et al does not teach the first solder paste is the first solder ball. Burnette

Art Unit: 2827

teaches a carrier substrate (320, Fig. 11) comprising a plurality of first solder balls (318) and the plurality of second solder balls (314). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to replace the plurality of first solder pastes of Dockerty et al by a plurality of first solder balls as taught by Burnette for providing good electrical and mechanical interconnection.

With respect to claims 9 and 14, Dockerty et al discloses a carrier substrate (1, Fig. 1) wherein the plurality of first solder paste (12) having a first dimension and the plurality of second solder balls (11) having a second dimension such that when heat, the heat having a temperature equal to the first melting temperature, and less than the second melting temperature, is applied to the solder ball array, only the plurality of first solder paste (12) are melted (see Figs. 1 and 2). It should be noted that: since the first solder paste (12) has the lower melting temperature than the second solder ball (11), thus only the first solder paste will be melted when the heat having a temperature equal to the first melting temperature. Dockerty et al does not teach the first solder paste is the first solder ball. Burnette teaches a carrier substrate (320, Fig. 11) comprising a plurality of first solder balls (318) and the plurality of second solder balls (314). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to replace the plurality of first solder pastes of Dockerty et al by a plurality of first solder balls as taught by Burnette for providing good electrical and mechanical interconnection.

With respect to claim 10, figure 1 of Dockerty et al further shows that integrated circuit (3) disposed on the bottom side of the carrier substrate (1).

With respect to claim 11, figure 1 of Dockerty et al shows that the application specific integrated circuit (3) is capable of being soldered to a printed circuit board (1), and the plurality of second solder balls (11) define an air gap between the printed circuit board and the application specific integrated circuit (3).

With respect to claim 12, figure 5 of Dockerty et al further shows that the carrier substrate (24) comprising at least one heat sink (27) disposed on a top surface of the carrier substrate.

With respect to claim 13, Dockerty et al discloses a carrier substrate (1, Fig. 1) wherein the plurality of second members (11) includes an outer layer of a solder material/first material having the first melting temperature (high melting temperature) (see col. 3, lines 57-60).

With respect to claim 17, as best understood, it recites limitations similar to claim 10. Dockerty et al further discloses the second solder balls (minimum dimension) (11, Fig. 1) is defined between the application specific integrated circuit (3) and the printed circuit board (1). Thus, claim 17 is rejected for the same reasons.

Method claims 23-26 are deemed to be inherent upon the references of Dockerty et al and Burnette as applied to claims 8-14.

Response to Arguments

6. Applicant's arguments filed 06/09/03 have been fully considered but they are not persuasive.

Applicant argued that the teaching of Matthies fails to teach or suggest the limitations directed to dispensing the second members in view of the teaching of Dockerty.

In response, the examiner disagrees with Applicant's argument because Dockerty teaches all limitations (as recited in claims 1, 15 and 21), except for the teaching of "a solder dispensing machine" which is applied to make/produce/generate first and second solder members. Matthies et al only teach the use of a dispensing machine 30 (see Fig. 2) which would be used to dispense bumps 14 (see Figs. 1-2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the prior art (reference) of Dockerty by using a dispensing machine as taught by Matthies in figure 2, in order to dispense/produce first and second solder members disposed on the carrier substrate. The combination of the teaching of Dockerty and Matthies would provide a very high rate of speed for making/producing/generating the solder members (for example, first and second solder members), thus this use of a dispensing machine will reduce the processing time of solder balls (see col. 2, lines 9-21 in Matthies's reference).

Additionally, the language of "disposed thereon with a solder dispensing machine" (as recited in claims 1 and 21) is an intended use language, it is not an invented matter and it has not been given patentable weight, since it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ F.2d 1647 (1987).

Applicant also argued that one of ordinary skill in the art would not be motivated to combine the references of Dockerty and Burnette because Dockerty teaches away from the solder paste being a plurality of solder balls. The examiner agrees with Applicant that Dockerty does not teach solder member 12 is in shape of a ball but a paste. However, Burnette teaches the

connection between a plurality of first solder balls and a plurality of second solder balls.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Dockerty by changing the shape of pastes 12 to become balls (solder balls) as taught by Burnette for interconnecting with the second solder balls to provide good electrical and mechanical solder balls interconnection. It should be noted that: since first solder pastes (12) and second solder balls (11) having different melting temperature, it does not matter the solder member is a solder paste or solder ball, solder ball can be pressed into the modified solder member 12 or solder ball 318 having "ball" shape (solder ball) as shown in figure 11 of Burnette.

Additionally, Appellants have presented **no argument** which convince us that the particular configuration of the solder member is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing good electrical and mechanical interconnection. See *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT


David A. Zanecke
Primary Examiner
AU 2827
2/20/14